AMENDMENTS TO THE CLAIMS:

Complete Claim Listing:

1. (Currently Amended) A method for multiplying a first signal and a second signal, comprising:

providing a substrate and a semiconductor structure over the substrate, the semiconductor structure having a first sidewall, a second sidewall, and a top surface;

depositing at least one substantially conformal layer over the substrate, wherein the at least one substantially conformal layer comprises at least a layer of gate material, wherein the at least one substantially conformal layer has a top surface at a height over the semiconductor structure;

forming a substantially planar layer over the substrate below the height of the top surface of the at least one substantially conformal layer over the semiconductor structure;

non-abrasively etching through the layer of gate material over the top surface of the semiconductor structure;

patterning the at least one substantially conformal layer to form a gate structure prior to the forming the substantially planar layer over the substrate, wherein the non-abrasive etching through the layer of gate material over the top surface of the semiconductor structure further includes etching through the layer of gate material of the gate structure over the top surface of the semiconductor structure to form a first gate portion and a second gate portion that are electrically isolated;

forming symmetrical source and drain regions relative to the first and second gate portions such that a channel region will be formed under the first and second gates during operation of the semiconductor structure;

applying the first signal to the first gate portion, wherein the first signal is time-varying; and

applying the second signal to the second gate portion, wherein the second signal is time-varying.

2. (Original) The method of claim 1, wherein the first gate portion has a portion running generally parallel to a surface of the substrate, the method further comprising forming a contact on the portion of the layer of gate material running generally parallel to the surface of the substrate for receiving the first mixer signal.

3. (Original) The method of claim 1, wherein forming the substantially planar layer comprises:

depositing material of the substantially planar layer to a height above the height of the top surface of the at least one substantially conformal layer; and

etching back the material of the substantially planar layer to a height below the height of the top surface of the at least one substantially conformal layer to expose the top surface of the at least one substantially conformal layer over the top surface of the semiconductor structure.

4. (Original) The method of claim 1, wherein the forming the substantially planar layer comprises depositing material of the substantially planar layer over a surface of the semiconductor substrate to a height below the height of the top surface of the at least one substantially conformal layer.

5. (Original) The method of claim 1, wherein forming the substantially planar layer comprises spinning on material of the substantially planar layer.

6. (Original) The method of claim 1, wherein the at least one substantially conformal layer further comprises a nitride layer over the layer of gate material.

7. (Original) The method of claim 6 further comprising:

etching through the nitride layer over the top surface of the semiconductor structure prior to the non-abrasive etching through the layer of gate material.

8. (Original) The method of claim 1 further comprising forming a dielectric layer on the semiconductor structure prior to forming the at least one substantially conformal layer.

9. (Original) The method of claim 1, wherein the first signal is an oscillator signal and the second signal is an analog signal.

10. (Original) The method of claim 1, wherein the first signal is an oscillator signal and the second signal is a digital signal.

11. (Original) The method of claim 1, wherein the substantially planar layer includes photo resist.

12. (Original) The method of claim 1, wherein the layer of gate material is selected from one of metal and polysilicon.

13. (Original) The method of claim 1, wherein the providing the substrate further comprises providing the semiconductor structure with a plurality of sources and drains, wherein the sources are connected together and the drains are connected together.

14. (Original) The method of claim 1, wherein the at least one conformal layer includes a second substantially conformal layer formed after the layer of gate material, the second substantially conformal material is for use as an etch stop layer.

15. (Original) The method of claim 1 further comprising:

providing a dielectric structure over the top surface of the semiconductor structure, the dielectric structure having a top surface, wherein the at least one substantially conformal layer is deposited over the dielectric structure, wherein the non-abrasive etching through the layer of gate material further includes etching through the layer of gate material over the top surface of the dielectric structure.

16. (Original) The method of claim 1, further comprising:

implanting dopants at a first angle relative to the substrate of a first type into the layer of gate material in an area adjacent to the first sidewall; and

implanting dopants at a second angle relative to the substrate of a second type into the layer of gate material in an area adjacent to the second sidewall.

17. (Currently Amended) A method of multiplying a first signal and a second signal, comprising:

providing a substrate having a semiconductor structure over the substrate, the semiconductor structure having a first sidewall, a second sidewall, and a top surface;

forming a first dielectric layer on the semiconductor structure;

depositing a first substantially conformal layer of gate material over the substrate after forming the first dielectric layer;

forming a second substantially conformal layer of a material different from the first substantially conformal layer over the first substantially conformal layer;

depositing a substantially planar layer over the substrate after depositing the second substantially conformal layer;

etching through the first substantially conformal layer and the second substantially conformal layer over the top surface of the semiconductor structure to result in a first portion of the first substantially conformal layer on the first sidewall of the semiconductor structure and extending over a first portion of the substrate and a second portion of the first substantially conformal layer on the second sidewall of the semiconductor structure and extending over a second portion of the substrate, wherein the first and second portions are electrically isolated from each other;

forming symmetrical source and drain regions relative to the first and second portions such that a channel region will be formed under the first and second gates during operation of the semiconductor structure;

applying the first signal to the first portion; and

applying the second signal to the second portion.

18. (Original) The method of claim 17, further comprising:

forming a first contact to the first portion of the first substantially conformal layer over the first portion of the substrate; and.

forming a second contact to the second portion of the first substantially conformal layer over the second portion of the substrate.

19. (Original) The method of claim 18, further comprising removing the second substantially conformal layer after the etching through the first substantially conformal layer and the etching through the second substantially conformal layer.

20. (Original) The method of claim 19, wherein the substantially planar layer is a spin-on material.

21. (Original) The method of claim 17, wherein the providing the substrate further comprises providing the semiconductor structure with a plurality of sources and drains, wherein the sources are connected together and the drains are connected together.

22. vThe method of claim 17, wherein the forming the substantially planar layer comprises depositing material of the substantially planar layer to a height lower than a height of a top surface of the second substantially conformal layer over the top surface of the semiconductor structure.

23. (Original) The method of claim 17, further comprising etching back the substantially planar layer to lower the substantially planar layer below a height of a top surface of the second substantially conformal layer over the semiconductor structure prior to etching through the first substantially conformal layer.

24. (Original) The method of claim 17, wherein the first signal is an oscillator signal and the second signal is analog.

25. (Original) The method of claim 17, wherein the first signal is an oscillator signal and the second signal is digital.

26. (Currently Amended) A method of forming a semiconductor structure, comprising:
providing a substrate;
forming a semiconductor fin on the substrate, the fin having first and second sidewalls;
forming a layer of gate material over the substrate and the fin, the gate material including a first portion adjacent to the first sidewall of the fin and a second portion adjacent the second sidewall of the fin;
removing the layer of gate material over the semiconductor fin to leave a first gate along the first sidewall and a second gate along the second sidewall, wherein the first and second gates are electrically isolated;
forming symmetrical source and drain regions relative to the first and second gates such that a channel region will be formed under the first and second gates during operation of the semiconductor structure;
applying a first signal to the first gate; and
applying a second signal to the second gate.

27. (Original) The method of claim 26, wherein the semiconductor fin has a plurality of fin portions separated by adjacent pairs of source contacts and drain contacts, wherein the source contacts are electrically connected together and the drain contacts are electrically connected together.

28. (Original) The method of claim 27, wherein the first gate comprises a first plurality of gate portions electrically connected together, wherein each of the gate portions of the first plurality of gate portions is adjacent to the first sidewall and between one of the adjacent pairs of source and drain contacts.

29. (Currently Amended) The method of claim ~~24~~ 26, wherein the first signal is an oscillator signal and the second signal is an analog signal.

30. (Currently Amended) The method of claim ~~24~~ 26, wherein the first signal is an oscillator signal and the second signal is a digital signal.

31. (Canceled) A multiplier circuit, comprising:

a substrate and a semiconductor structure over the substrate, the semiconductor structure comprising a first sidewall, a second sidewall, and a top surface;

a first continuous layer of a conformal material comprising a first portion along the first sidewall and a second portion extending substantially parallel to the substrate from the first portion, wherein the first portion is a first gate and the second portion is a first contact region,

a first contact on the first contact region for receiving a first signal;

a second continuous layer of the conformal material comprising a third portion along the second sidewall and a fourth portion extending substantially parallel to the substrate from the third portion, wherein the third portion is a second gate, the second portion is a second contact region, and the first gate and the second gate are electrically isolated from each other; and

a second contact on the second contact region for receiving the second signal.

32. (Canceled) The multiplier circuit of claim 31, wherein the semiconductor structure comprises a plurality of fin portions separated by adjacent pairs of source contacts and drain contacts, wherein the source contacts are electrically connected together and the drain contacts are electrically connected together.

33. (Canceled) The multiplier circuit of claim 32, wherein the first gate comprises a first plurality of gate portions electrically connected together, wherein each of the gate portions of the first plurality of gate portions is adjacent to the first sidewall and between one of the adjacent pairs of source and drain contacts.

34. (Canceled) The multiplier circuit of claim 31, wherein the semiconductor structure comprises a plurality of alternating source and drain contacts and wherein the first gate

comprises a first gate portion between each source and drain contact adjacent to the first sidewall and the second gate comprises a second portion between each source and drain contact adjacent to the second sidewall.

35. (Canceled) The multiplier circuit of claim 34, wherein the multiplier circuit is a phase detector.

36. (Canceled) The multiplier circuit of claim 31, wherein the semiconductor structure comprises a plurality of alternating source and drain contacts and wherein the first gate comprises a first gate portion between each source and drain contact adjacent to the first sidewall and the second gate comprises a second portion between each source and drain contact adjacent to the second sidewall.

37. (Canceled) The multiplier circuit of claim 31, further comprising

a second semiconductor structure over the substrate, the second semiconductor structure comprising a third sidewall, a fourth sidewall, and a second top surface;

a third continuous layer of a conformal material comprising a fifth portion along the third sidewall and a sixth portion extending substantially parallel to the substrate from the fifth portion, wherein the fifth portion is a third gate and the sixth portion is a third contact region,

a third contact on the third contact region for receiving a third signal;

a fourth continuous layer of the conformal material comprising a seventh portion along the fourth sidewall and an eighth portion extending substantially parallel to the substrate from the seventh portion, wherein the seventh portion is a fourth gate, the eighth portion is a fourth contact region, and the third gate and the fourth gate are electrically isolated from each other; and

a fourth contact on the eighth contact region for receiving a fourth signal.

38. (Canceled) The multiplier circuit of claim 37, wherein the first and second sidewalls are separated by a first thickness and the third and fourth sidewalls are separated by a second thickness different from the first thickness.

39. (Canceled) The multiplier circuit of claim 37, wherein the semiconductor structure comprises adjacent source and drain contacts separated by a first distance and the second semiconductor structure comprises adjacent source and drain contacts separated by a second distance that is different than the first distance.

40. (Canceled) The multiplier circuit of claim 37, wherein the first signal is an oscillator signal and the second signal is a digital signal.

41. (Canceled) The multiplier circuit of claim 37, wherein the first signal is an oscillator signal and the second signal is an analog signal.